REMARKS

Claims 1, 3, 5 – 10, and 12 are pending. Claims 2, 4, and 11 have been cancelled. Claim 12 has been added. Claims 1, 6, 7, 9, and 10 have been amended. No new matter has been introduced. Reexamination and reconsideration of the application is respectfully requested.

In the March 1, 2006 Office Action, the Examiner object to Fig. 5 because Fig. 5 did not have a legend designating the drawing as prior art. The applicant have submitted a replacement sheet identifying Fig. 5 as prior art. The applicant respectfully requests that the objections to the drawings be withdrawn.

In the March 1, 2006 Office Action, the Examiner rejected claims 3 and 4 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. The Examiner noted that claims 3 and 4 did not provide any detail how the size of the register is set. *(Office Action, page 3)*. The applicant has cancelled claims 3 and 4. The Examiner also rejected claim 11 under 35 U.S.C. § 112, second paragraph, as being indefinite. *(Office Action, page 4)*. The applicant has also cancelled claim 11. The applicant notes that the rejections of claims 3, 4, and 11 are now moot due to the applicant's cancellation of the claims.

In the March 1, 2006 Office Action, the Examiner rejected claims 1 – 11 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 6,816,921 to Jahnke ("the Jahnke reference"). This rejection is respectfully traversed.

Claim 1 distinguishes over the cited references. Claim 1, as amended, recites:

> A data transfer control device for controlling data transfer between a first memory having a predetermined storage capacity and a second memory corresponding to a buffer memory incorporated in a peripheral module, said data transfer control device comprising:

a first register for storing a first value representing a first number of times, by which data transfer is performed from the first memory to the second memory, the first value being determined based on a number of bits of data being output from the first memory and a storage capacity of the second memory;

a second register for storing a second value representing a second number of times by which data transfer is performed from the first memory to the second memory, the second value being determined based on an amount of data being stored in the first memory and being transferred to the second memory and the number of bits of data being output from the first memory; and

a controller for controlling the data transfer from the first memory to the second memory in accordance with the first value and for outputting an interrupt signal when a value accumulating the number of times data transfer is performed from the first memory to the second memory matches the second value.

The Jahnke reference does not disclose, teach, or suggest the data transfer control device of claim 1, as amended. The Examiner states that the Jahnke reference discloses a first register (i.e., the target word size register (the TWS register) for storing a first value representing a first number of times for performing data transfer to suit a storage capacity of the second memory. *(Office Action, page 5)*. Specifically, the Jahnke reference discloses a microcontroller DMA unit for transferring data from a source to a target. In the Jahnke reference, the number of words being transferred is determined by the value stored in the CNTVAL counter. The count value in the CNTVAL register decrements every time one-word data transfer is completed, so that when the count value of the CNTVAL register is reduced to zero, the DMA transfer is completed. The TWS register indicates the value representing the word size of the target, which the user can arbitrarily set, e.g., 8 bits, 16 bits, or 32 bits per word. The TWS register establishes the number of bits in one word. *(Jahnke, col. 5, lines 20 – 32, and col. 6, lines 28 – 42)*.

This is not the same as a data transfer control device for controlling data transfer

between a first memory having a predetermined storage capacity and a second memory corresponding to a buffer memory incorporated in a peripheral module including **a first register for storing a first value representing a first number of times, by which data transfer is performed from the first memory to the second memory, the first value being determined based on a number of bits of data being output from the first memory and a storage capacity of the second memory,** as is recited in claim 1, as amended. It is not the same because the Jahnke reference's TWS register is utilizing only the word size for the target location. The TWS register is not utilizing a number of times by which data transfer is to be performed, the TWS register is utilized so that the microcontroller DMA is to write data to the target location as defined by this word size. Thus, the Jahnke reference is not disclosing that **the first value (or first number of times) is determined based on a number of bits being output from the first memory and a storage capacity of the second memory**, as is recited in claim 1, as amended. The number of bits being output from the first memory does not factor into the value in the TWS register of the Jahnke reference because the Jahnke TWS value is determined based on what the bus is able to support (i.e., what the Advance High Performance Bus (AHB) of the Jahnke reference). Similarly, the storage capacity of the second memory in the Jahnke reference, does not factor into the determination of the value in the TWS register. Accordingly, applicant respectfully submits that claim 1, as amended, distinguishes over the Jahnke reference.

Claim 7, as amended, recites limitations similar to claim 1, as amended. Accordingly, applicant respectfully submits that claim 7 distinguishes over the Jahnke reference for reasons similar to those discussed above in regard to claim 1, as

amended.

Claims 2, 5, 6, 8 – 10, and 12 depend, indirectly or directly, on claims 1 and 7. Accordingly, applicant respectfully submits that claims 2, 5, 6, 8 – 10 and 12 distinguish over the Jahnke reference for the same reasons as those discussed above with regard to claim 1.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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Date: July 3, 2006

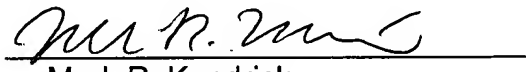
By: 

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FIG. 5
(Prior Art)